SIMULTANEOUS TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS
SIMULTANEOUS TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS

• Genetic programming can simultaneously create a circuit's topology and sizing along with the placement and routing of all components as part of an integrated one-pass design process.

• It can do this while also optimizing additional other considerations (such as minimizing the circuit's area).
AUTOMATIC TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS

- The topology of a circuit includes specifying the gross number of components in the circuit, the type of each component (e.g., a capacitor), and a netlist specifying where each lead of each component is to be connected.

- Sizing involves specifying the values (typically numerical) of each of the circuit's components.
AUTOMATIC TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS — CONTINUED

• *Placement* involves the assignment of each of the circuit's components to a particular physical location on a printed circuit board or silicon wafer.

• *Routing* involves the assignment of a particular physical location to the wires between the leads of the circuit's components.
LAYOUT — CONTINUED

- This is accomplished by using an initial circuit that contains information about the geographic (physical) location of components and wires on a silicon chip or on a particular side of a printed circuit board.

- Also, component-inserting and topology-modifying operations appropriately adjust the geographic (physical) location of all inserted or affected components and wires.
LAYOUT — CONTINUED

- Initial circuit complies with the requirements that
  - wires must not cross on a particular layer of a silicon chip or on a particular side of a printed circuit board,
  - there must be a wire connecting 100% of the leads of all the circuit's components,
  - minimum clearance distances between wires, between components, and between wires and components must be respected.

- Each circuit-constructing function preserves compliance with these requirements. So fully laid-out circuit also complies
LAYOUT — ONE-INPUT, ONE-OUTPUT INITIAL CIRCUIT FOR A LOWPASS FILTER

- Each element is of a particular size and is located at a particular geographic (physical) location.
INITIAL CIRCUIT — CONTINUED

- Source point $V$ and output probe point $O$ each occupy $1 \times 1$ area
- Nonmodifiable wires each occupy $1 \times n$ or $n \times 1$ area
- Modifiable wires each occupy $1 \times 1$ area
- Resistors, capacitors, and inductors each occupy $3 \times 3$ area
PARTIAL CIRCUIT WITH A $1 \times 1$ PIECE OF MODIFIABLE WIRE $Z_0$ AT LOCATION (20, 20) AND FOUR CAPACITORS
The application of the **LAYOUT–C** function to the modifiable wire Z0 causes a $3 \times 3$ capacitor C6 to be inserted at location (20, 20).

- The insertion of the new capacitor C6 forces a change in location for the other capacitors.
The application of LAYOUT–CMOS–TRANSISTOR function to the modifiable wire \( Z_0 \) causes a three-leaded transistor \( Q_6 \) occupying a \( 3 \times 3 \) area to be inserted at location \((18, 20)\).
The application of the **SERIES–LAYOUT** function to the modifiable capacitor C6 causes a new $3 \times 3$ capacitor C8 to be inserted at location (22, 20) in series with C6.
PARALLEL-LAYOUT-LEFT FUNCTION

PARALLEL-LAYOUT-RIGHT FUNCTION
• The application of the VIA–TO–GROUND–NEG–LEFT–LAYOUT function to the modifiable capacitor C₆ causes a new 1 x 1 connection to ground G to be inserted at location (20, 24).
LAYOUT
LOWPASS FILTER

TWO-SIDED PRINTED CIRCUIT BOARD

FUNCTION AND TERMINALS

\[ \mathcal{F}_{\text{CCS}} = \{ \text{C-LAYOUT, L-LAYOUT, SERIES-LAYOUT, PARALLEL-LAYOUT-LEFT, PARALLEL-LAYOUT-RIGHT, FLIP, NOOP, VIA-TO-GROUND-NEG-LEFT-LAYOUT, VIA-TO-GROUND-NEG-RIGHT-LAYOUT, VIA-TO-GROUND-POS-LEFT-LAYOUT, VIA-TO-GROUND-POS-RIGHT-LAYOUT} \} \]
• The terminal set, \( \mathcal{T}_{ccs} \), for each construction-continuing subtree:
  \( \mathcal{T}_{ccs} = \{ \text{END} \} \).

• The terminal set, \( \mathcal{T}_{aps} \), for each arithmetic-performing subtree:
  \( \mathcal{T}_{aps} = \{ \Re \} \).

• The function set, \( \mathcal{F}_{aps} \), for each arithmetic-performing subtree:
  \( \mathcal{F}_{aps} = \{ +, - \} \).
LAYOUT
LOWPASS FILTER
FITNESS MEASURE

• Two-part fitness measure
• The first term is the sum, over the 101 fitness cases (sampled frequencies), of the absolute weighted deviation between the actual value of the voltage that is produced by the circuit at the probe point $V_{OUT}$ and the target value for voltage (0 or 1 volts).
• The second term is the area of the bounding rectangle for the fully developed circuit divided by 100,000 square units of area.
LAYOUT
LOWPASS FILTER
FITNESS MEASURE
— CONTINUED

• The term involving the bounding rectangle is much smaller than the term involving the filter's frequency response until a circuit scores 101 (or near 101) hits. For individuals not scoring the maximum number (101) of hits, fitness is the sum of the two terms. For individuals scoring the maximum number of hits, fitness is only the area-based term.

• Unsimulatable circuits — High penalty value of 10^8
LAYOUT — LOWPASS FILTER —
RESULTS

BEST OF GENERATION 0
Contains two inductors (L2 and L11) and two capacitors (C10 and C19) in addition to all of the nonmodifiable elements of the original test fixture of the initial circuit.
LAYOUT — LOWPASS FILTER —
RESULTS — CONTINUED

FREQUENCY DOMAIN BEHAVIOR OF
BEST CIRCUIT FROM GENERATIONS 0,
8, AND 25
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

BEST CIRCUIT OF GENERATION 8 CONTAINING FIVE INDUCTORS AND THREE CAPACITORS
100%-COMPLIANT BEST CIRCUIT OF GENERATION 25 CONTAINING FIVE CAPACITORS AND 11 INDUCTORS (TOTAL OF 16 COMPONENTS) OCCUPying AN AREA OF 1775.2
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

100%-COMPLIANT BEST CIRCUIT OF GENERATION 30 CONTAINING 10 INDUCTORS AND FIVE CAPACITORS (TOTAL OF 15 COMPONENTS) OCCUPYING AN AREA OF 950.3
100%-COMPLIANT BEST-OF-RUN CIRCUIT OF GENERATION 138 CONTAINING FOUR INDUCTORS AND FOUR CAPACITORS (TOTAL OF ONLY EIGHT COMPONENTS) OCCUPYING AN AREA OF 359.4
## LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

### COMPARISON OF THREE BEST-OF-GENERATION CIRCUITS SCORING 101 HITS

<table>
<thead>
<tr>
<th>Gen</th>
<th>Number of Capacitors</th>
<th>Number of Inductors</th>
<th>Number of Shunts</th>
<th>Area Frequency-Based Term</th>
<th>Fitness</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>5</td>
<td>11</td>
<td>4</td>
<td>1775.2</td>
<td>0.264698</td>
</tr>
<tr>
<td>30</td>
<td>10</td>
<td>5</td>
<td>4</td>
<td>950.3</td>
<td>0.106199</td>
</tr>
<tr>
<td>138</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>359.4</td>
<td>0.193066</td>
</tr>
</tbody>
</table>
AUTOMATIC SYNTHESIS, PLACEMENT, AND ROUTING OF A 60 DB AMPLIFIER CIRCUIT (USING TRANSISTORS)
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — CONTINUED

THE INITIAL CIRCUIT
• Three modifiable wires, $Z_0$, $Z_1$, and $Z_2$
• Two ground points $G$
• Input point $V$
• Output point $O$
• Nonmodifiable wire (hashed)
• Fixed 1 kilo-Ohm ($k\Omega$) source resistor $R_4$
• Fixed 1 $k\Omega$ load resistor $R_{18}$
• Fixed 1 giga-Ohm feedback resistor $R_{14}$
• Fixed 999 $\Omega$ balancing resistor $R_3$. 
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — FITNESS

- Fitness is the sum of the area of the bounding rectangle for the fully developed and laid-out circuit divided by 1,000,000 plus the amplification penalty, bias penalty, and two non-linearity penalties; however, if this sum is less than 0.1 (indicating a good amplifier), the fitness becomes simply the rectangle's area divided by 1,000,000.

- Population size, \( M \), is 10,000,000
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

- The first best-of-generation circuit delivering 60 dB of amplification appears in generation 65.
- This 27-component circuit occupies an area of 8,234 and has overall fitness of 33.042583.
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

BEST-OF-RUN CIRCUIT FROM GENERATION 101
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

COMPARISON OF BEST-OF-GENERATION CIRCUITS FROM GENERATIONS 65 AND 101

<table>
<thead>
<tr>
<th>Gen</th>
<th>Components</th>
<th>Area</th>
<th>Four penalties</th>
<th>Fitness</th>
</tr>
</thead>
<tbody>
<tr>
<td>65</td>
<td>27</td>
<td>8,234</td>
<td>33.034348</td>
<td>33.042583</td>
</tr>
<tr>
<td>101</td>
<td>19</td>
<td>4,751</td>
<td>0.061965</td>
<td>0.004751</td>
</tr>
</tbody>
</table>
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

BEST CIRCUIT OF GENERATION 101

X AND Y COORDINATES FOR OF THE 19 COMPONENTS, COMPONENT VALUE (SIZING) FOR EACH CAPACITOR AND RESISTOR, THE TYPE (NPN Q2N3904 OR PNP Q2N3904) FOR EACH TRANSISTOR

<table>
<thead>
<tr>
<th>Component</th>
<th>X coordinate</th>
<th>Y coordinate</th>
<th>Sizing / Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q8</td>
<td>-8.398678</td>
<td>21.184582</td>
<td>q2n3906</td>
</tr>
<tr>
<td>C10</td>
<td>-8.54565</td>
<td>31.121107</td>
<td>1.01e+02nf</td>
</tr>
<tr>
<td>R21</td>
<td>18.245857</td>
<td>-24.687471</td>
<td>1.48e+03k</td>
</tr>
<tr>
<td>R24</td>
<td>12.105233</td>
<td>-20.687471</td>
<td>5.78e+03k</td>
</tr>
<tr>
<td>R27</td>
<td>12.105233</td>
<td>-12.690355</td>
<td>3.61e+03k</td>
</tr>
<tr>
<td>R30</td>
<td>5.128666</td>
<td>-8.690355</td>
<td>8.75e+01k</td>
</tr>
<tr>
<td>R33</td>
<td>-3.398678</td>
<td>-4.690355</td>
<td>1.16e+03k</td>
</tr>
<tr>
<td>Q36</td>
<td>-3.398678</td>
<td>3.30961</td>
<td>q2n3906</td>
</tr>
<tr>
<td>Q39</td>
<td>-3.398678</td>
<td>13.309582</td>
<td>q2n3906</td>
</tr>
<tr>
<td>Q43</td>
<td>-18.472164</td>
<td>8.309597</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q45</td>
<td>-18.472164</td>
<td>-1.690355</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q46</td>
<td>-3.398678</td>
<td>21.184582</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q47</td>
<td>5.128666</td>
<td>21.184582</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q48</td>
<td>-18.472164</td>
<td>-17.687471</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q49</td>
<td>12.105233</td>
<td>21.184582</td>
<td>q2n3904</td>
</tr>
<tr>
<td>Q50</td>
<td>18.245857</td>
<td>21.184582</td>
<td>q2n3904</td>
</tr>
<tr>
<td>C52</td>
<td>-15.472164</td>
<td>31.121107</td>
<td>1.25e-01nf</td>
</tr>
<tr>
<td>C53</td>
<td>-15.472164</td>
<td>21.184582</td>
<td>7.78e+03nf</td>
</tr>
<tr>
<td>Q54</td>
<td>24.873787</td>
<td>31.121107</td>
<td>q2n3906</td>
</tr>
</tbody>
</table>