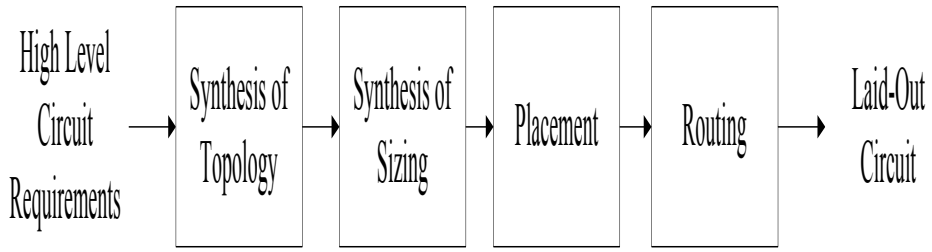
SIMULTANEOUS TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS

SIMULTANEOUS TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS

- **Genetic programming can simultaneously create a circuit's topology and sizing *along with the placement and routing* of all components as part of *an integrated one-pass design process*.**

- **It can do this while also optimizing additional other considerations (such as minimizing the circuit's area).**

AUTOMATIC TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS



- **The *topology* of a circuit includes specifying the gross number of components in the circuit, the type of each component (e.g., a capacitor), and a *netlist* specifying where each lead of each component is to be connected.**

- ***Sizing* involves specifying the values (typically numerical) of each of the circuit's components.**

AUTOMATIC TOPOLOGY, SIZING, PLACEMENT, AND ROUTING OF CIRCUITS — CONTINUED

• *Placement* involves the assignment of each of the circuit's components to a particular physical location on a printed circuit board or silicon wafer.

• *Routing* involves the assignment of a particular physical location to the wires between the leads of the circuit's components.

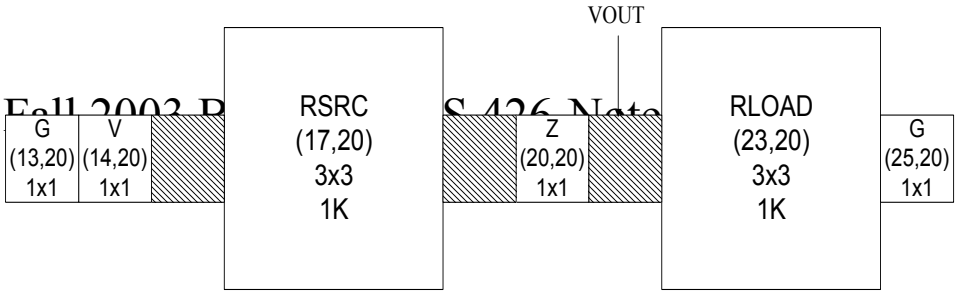
LAYOUT — CONTINUED

- **This is accomplished by using an initial circuit that contains information about the geographic (physical) location of components and wires a silicon chip or on a particular side of a printed circuit board**

- **Also, component-inserting and topology-modifying operations appropriately adjust the geographic (physical) location of all inserted or affected components and wires.**

LAYOUT — CONTINUED

- **Initial circuit complies with the requirements that**
  - **wires must not cross on a particular layer of a silicon chip or on a particular side of a printed circuit board,**
  - **there must be a wire connecting 100% of the leads of all the circuit's components,**
  - **minimum clearance distances between wires, between components, and between wires and components must be respected.**
- **Each circuit-constructing function preserves compliance with these requirements. so fully laid-out circuit also complies**



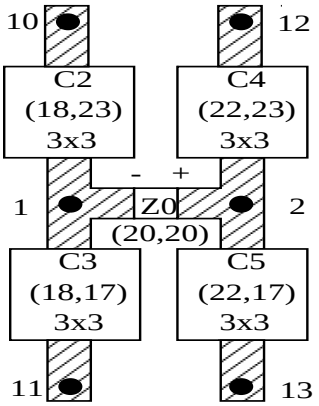
LAYOUT — ONE-INPUT, ONE-OUTPUT INITIAL CIRCUIT FOR A LOWPASS FILTER

- **Each element is of a particular size and is located at a particular geographic (physical) location.**

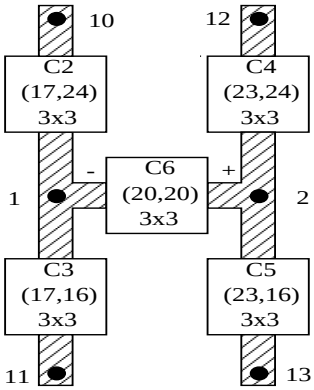
INITIAL CIRCUIT — CONTINUED

- **Source point V and output probe point O each occupy 1 × 1 area**
- **Nonmodifiable wires each occupy 1 × *n* or *n* × 1 area**
- **Modifiable wires each occupy 1 × 1 area**
- **Resistors, capacitors, and inductors each occupy 3 × 3 area**

PARTIAL CIRCUIT WITH A 1 × 1 PIECE OF MODIFIABLE WIRE Z0 AT LOCATION (20, 20) AND FOUR CAPACITORS

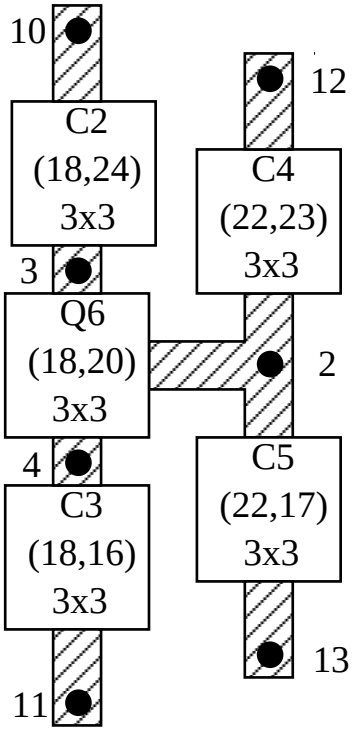


LAYOUT-C FUNCTION



- **The application of the LAYOUT-C function to the modifiable wire Z0 causes a 3 × 3 capacitor C6 to be inserted at location (20, 20).**
- **The insertion of the new capacitor C6 forces a change in location for the other capacitors.**

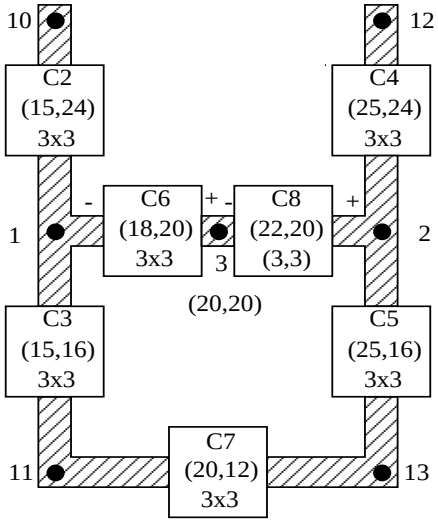
LAYOUT-CMOS-TRANSISTOR FUNCTION



- **The application of LAYOUT-CMOS-TRANSISTOR function to the modifiable wire Z0 causes a three-leaded transistor Q6 occupying a 3 × 3 area to be inserted at location (18, 20).**

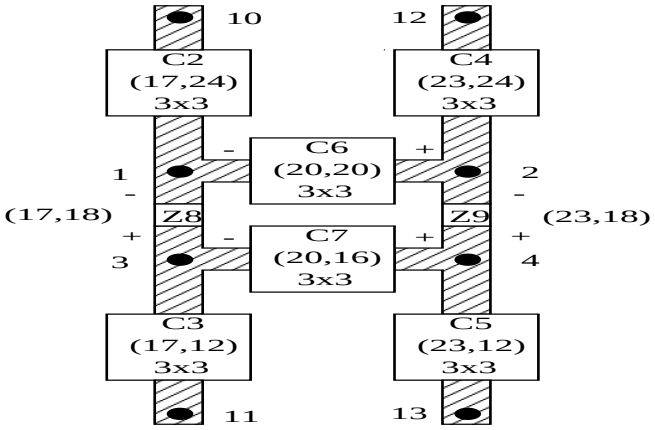
SERIES-LAYOUT FUNCTION

PARTIAL CIRCUIT WITH A 3 × 3 MODIFIABLE CAPACITOR C6 AT LOCATION (20, 20) WITH FIVE NEARBY CAPACITORS

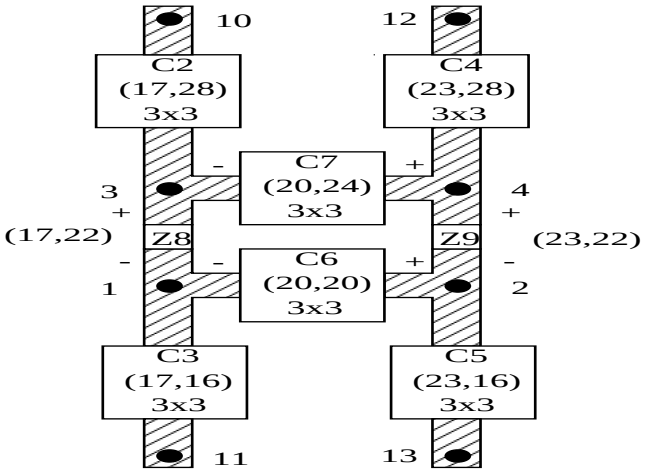


- **The application of the SERIES-LAYOUT function to the modifiable capacitor C6 causes a new 3 × 3 capacitor C8 to be inserted at location (22, 20) in series with C6.**

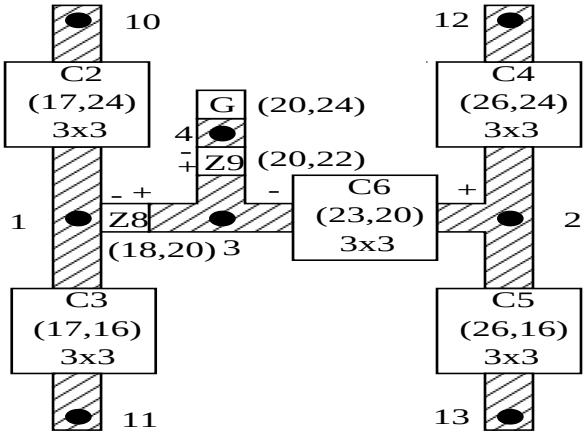
PARALLEL-LAYOUT-LEFT FUNCTION



PARALLEL-LAYOUT-RIGHT FUNCTION



VIA-TO-GROUND-NEG-LEFT-LAYOUT FUNCTION



- **The application of the VIA-TO-GROUND-NEG-LEFT-LAYOUT function to the modifiable capacitor C6 causes a new 1×1 connection to ground G to be inserted at location (20, 24).**

LAYOUT
LOWPASS FILTER

TWO-SIDED PRINTED CIRCUIT BOARD

FUNCTION AND TERMINALS

$\mathcal{F}_{CCS}$ = {**C-LAYOUT**, **L-LAYOUT**, **SERIES-LAYOUT**, **PARALLEL-LAYOUT-LEFT**, **PARALLEL-LAYOUT-RIGHT**, **FLIP**, **NOOP**, **VIA-TO-GROUND-NEG-LEFT-LAYOUT**, **VIA-TO-GROUND-NEG-RIGHT-LAYOUT**, **VIA-TO-GROUND-POS-LEFT-LAYOUT**, **VIA-TO-GROUND-POS-RIGHT-LAYOUT**}

LAYOUT
LOWPASS FILTER
FUNCTION AND TERMINALS — CONTINUED

- **The terminal set, $\mathcal{T}_{ccs}$, for each construction-continuing subtree:**

$\mathcal{T}_{ccs}$ = {END}.

- **The terminal set, $\mathcal{T}_{aps}$, for each arithmetic-performing subtree:**

$\mathcal{T}_{aps}$ = {$\Re$},

- **The function set, $\mathcal{F}_{aps}$, for each arithmetic-performing subtree:**

$\mathcal{F}_{aps}$ = {+, -}.

LAYOUT
LOWPASS FILTER
FITNESS MEASURE

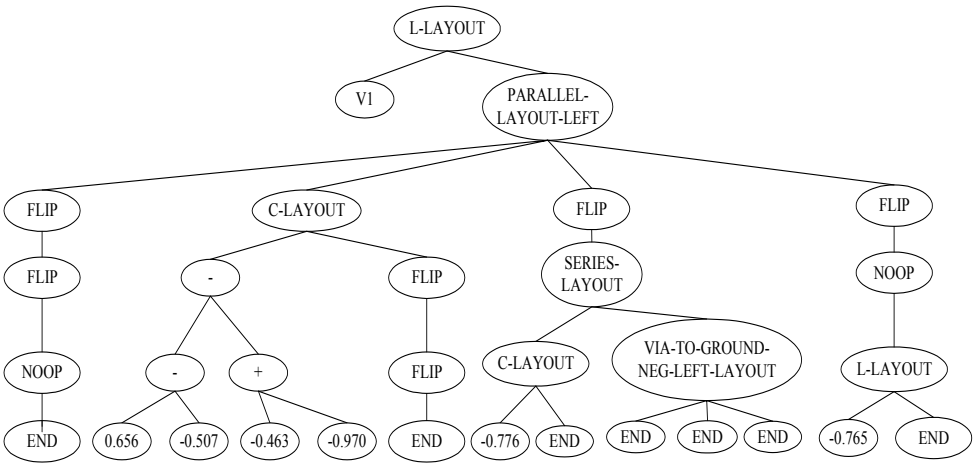
- **Two-part fitness measure**
- **The first term is the sum, over the 101 fitness cases (sampled frequencies), of the absolute weighted deviation between the actual value of the voltage that is produced by the circuit at the probe point VOUT and the target value for voltage (0 or 1 volts).**
- **The second term is the area of the bounding rectangle for the fully developed circuit divided by 100,000 square units of area.**

LAYOUT
LOWPASS FILTER
FITNESS MEASURE
— CONTINUED

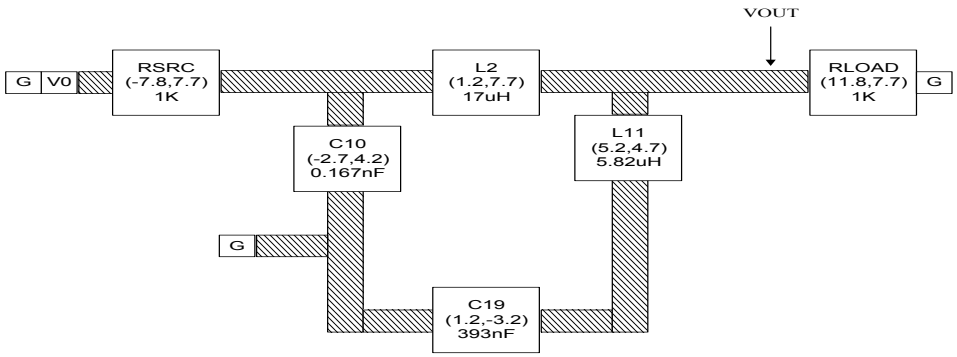
- **The term involving the bounding rectangle is much smaller than the term involving the filter's frequency response until a circuit scores 101 (or near 101) hits. For individuals not scoring the maximum number (101) of hits, fitness is the sum of the two terms. For individuals scoring the maximum number of hits, fitness is only the area-based term.**
- **Unsimulatable circuits — High penalty value of 10^8**

LAYOUT — LOWPASS FILTER — RESULTS

BEST OF GENERATION 0



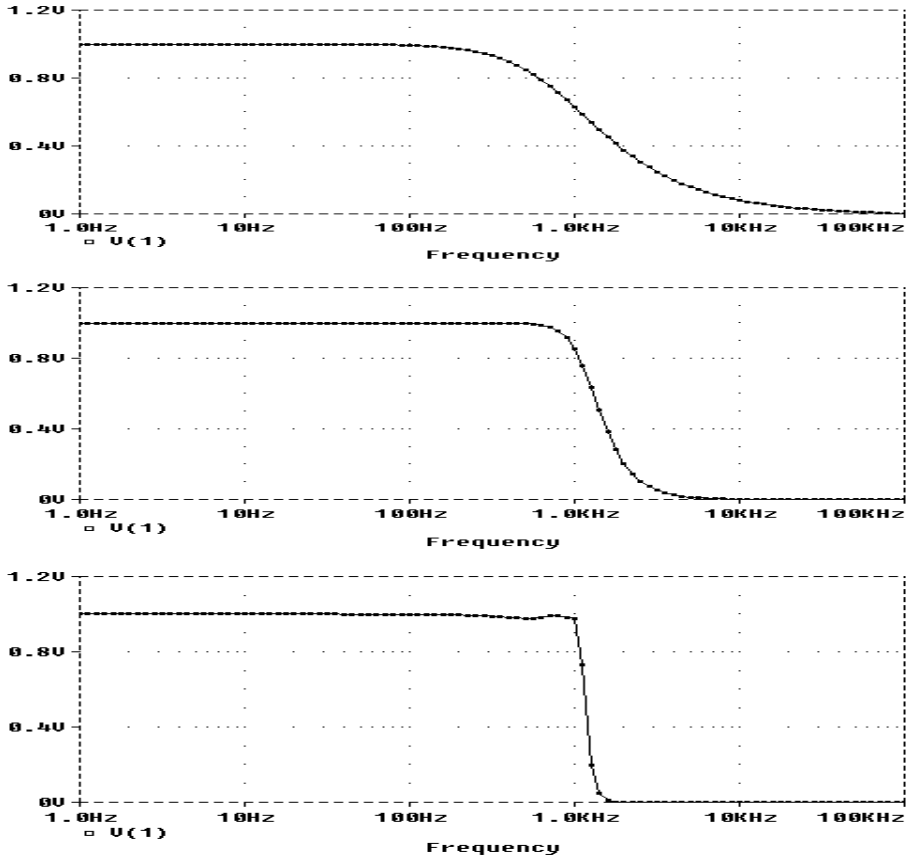
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED



- **Contains two inductors (L2 and L11) and two capacitors (C10 and C19) in addition to all of the nonmodifiable elements of the original test fixture of the initial circuit.**

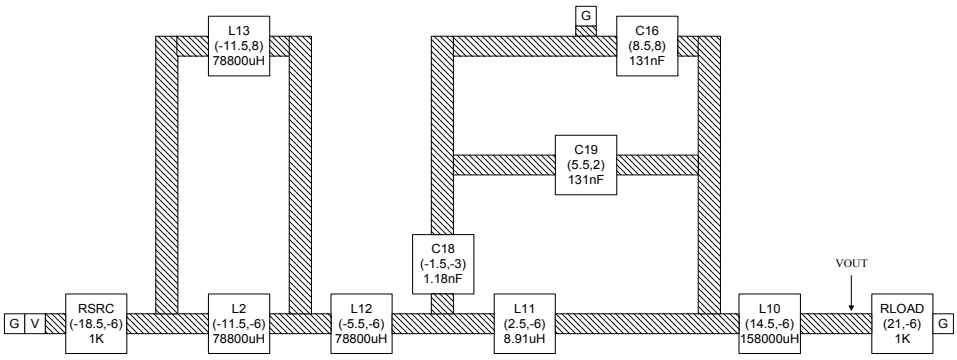
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

FREQUENCY DOMAIN BEHAVIOR OF BEST CIRCUIT FROM GENERATIONS 0, 8, AND 25



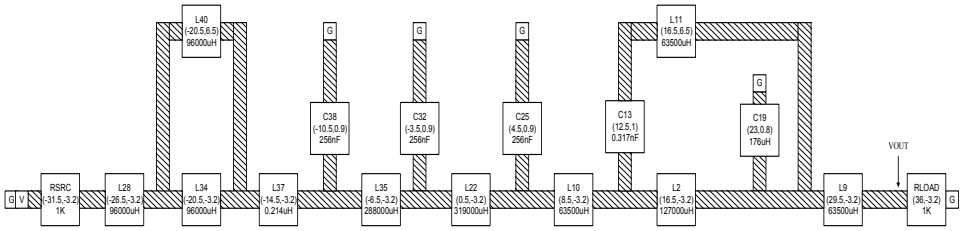
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

BEST CIRCUIT OF GENERATION 8 CONTAINING FIVE INDUCTORS AND THREE CAPACITORS



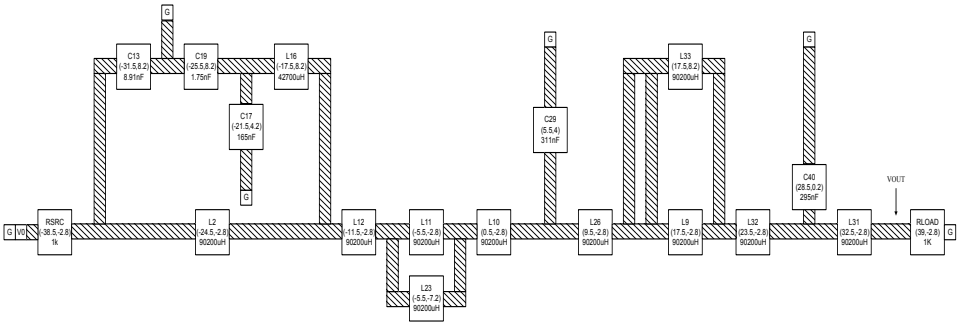
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

100%-COMPLIANT BEST CIRCUIT OF GENERATION 25 CONTAINING FIVE CAPACITORS AND 11 INDUCTORS (TOTAL OF 16 COMPONENTS) OCCUPYING AN AREA OF 1775.2



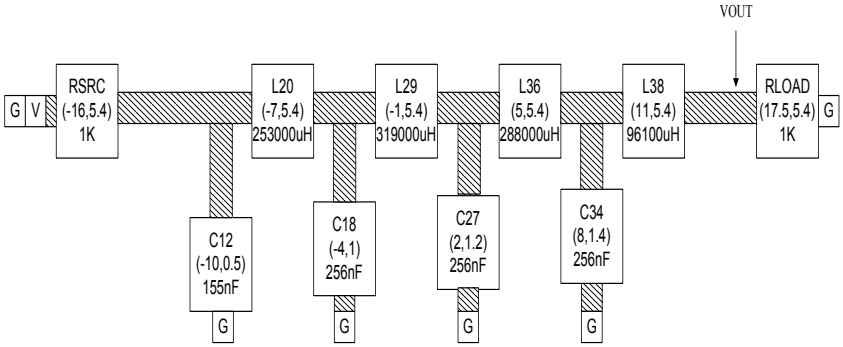
LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

100%-COMPLIANT BEST CIRCUIT OF GENERATION 30 CONTAINING 10 INDUCTORS AND FIVE CAPACITORS (TOTAL OF 15 COMPONENTS) OCCUPYING AN AREA OF 950.3



LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

100%-COMPLIANT BEST-OF-RUN CIRCUIT OF GENERATION 138 CONTAINING FOUR INDUCTORS AND FOUR CAPACITORS (TOTAL OF ONLY EIGHT COMPONENTS) OCCUPYING AN AREA OF 359.4

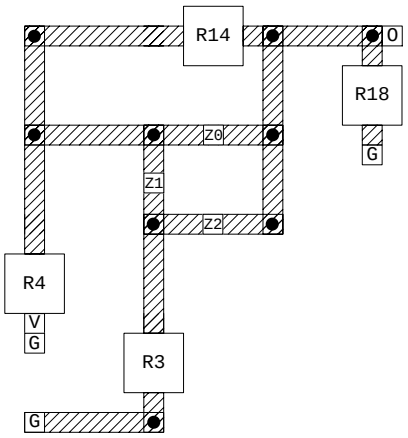


LAYOUT — LOWPASS FILTER — RESULTS — CONTINUED

COMPARISON OF THREE BEST-OF-GENERATION CIRCUITS SCORING 101 HITS

Gen	Number of Capacitors	Number of Inductors	Number of Shunts	Area	Frequency-Based Term	Fitness
25	5	11	4	1775.2	0.264698	0.01775
30	10	5	4	950.3	0.106199	0.00950
138	4	4	4	359.4	0.193066	0.00359

AUTOMATIC SYNTHESIS, PLACEMENT, AND ROUTING OF A 60 DB AMPLIFIER CIRCUIT (USING TRANSISTORS)



LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — CONTINUED

THE INITIAL CIRCUIT

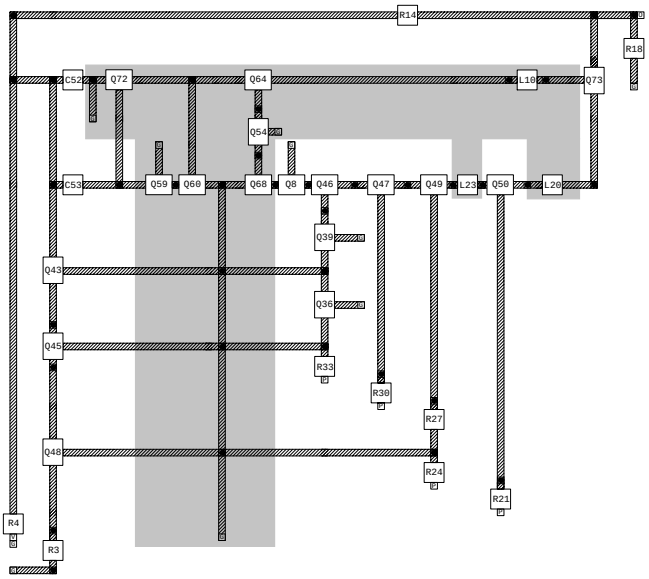
- Three modifiable wires, Z0, Z1, and Z2
- Two ground points G
- Input point V
- Output point O
- Nonmodifiable wire (hashed)
- Fixed 1 kilo-Ohm (kΩ) source resistor R4
- Fixed 1 kΩ load resistor R18
- Fixed 1 giga-Ohm feedback resistor R14
- Fixed 999 Ω balancing resistor R3.

LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — FITNESS

- **Fitness is the sum of the area of the bounding rectangle for the fully developed and laid-out circuit divided by 1,000,000 plus the amplification penalty, bias penalty, and two non-linearity penalties; however, if this sum is less than 0.1 (indicating a good amplifier), the fitness becomes simply the rectangle's area divided by 1,000,000.**

- **Population size, *M*, is 10,000,000**

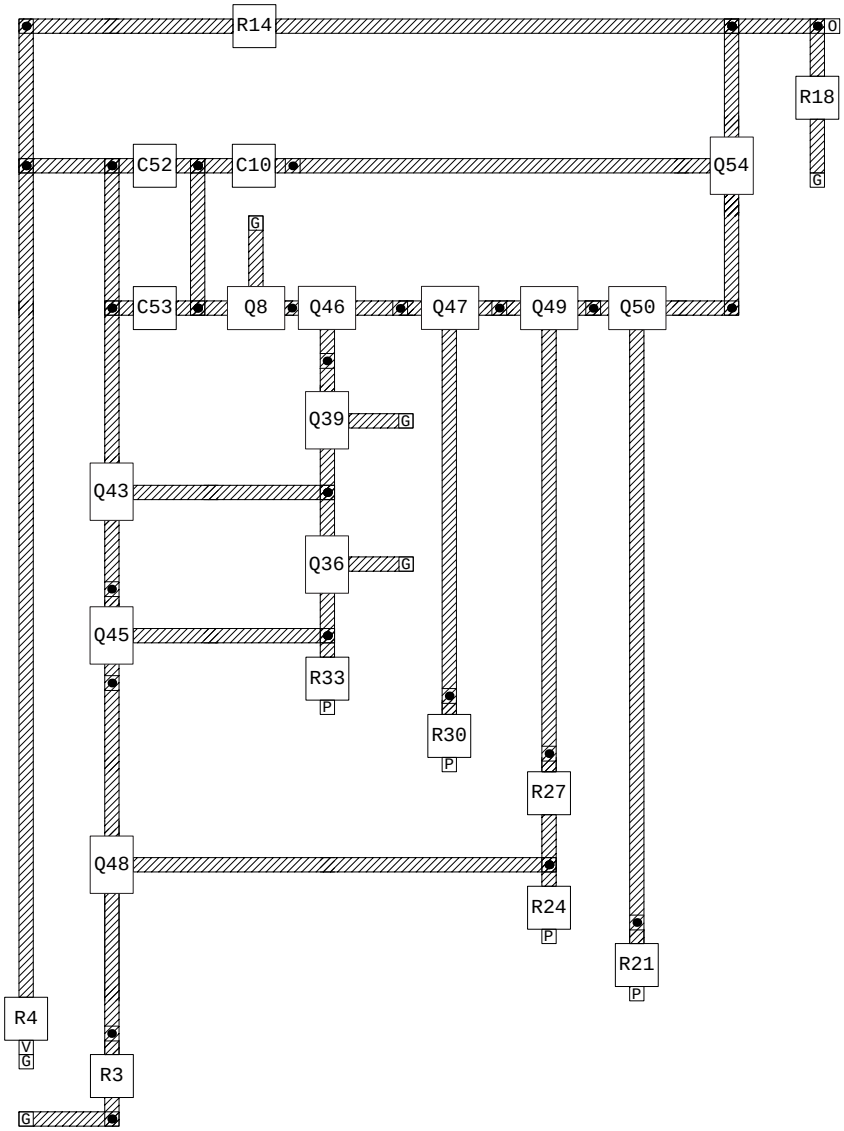
LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS



- **The first best-of-generation circuit delivering 60 dB of amplification appears in generation 65.**
- **This 27-component circuit occupies an area of 8,234 and has overall fitness of 33.042583.**

LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

BEST-OF-RUN CIRCUIT FROM GENERATION 101



LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

COMPARISON OF BEST-OF-GENERATION CIRCUITS FROM GENERATIONS 65 AND 101

Gen	Components	Area	Four penalties	Fitness
65	27	8,234	33.034348	33.042583
101	19	4,751	0.061965	0.004751

LAYOUT — 60 DB AMPLIFIER (USING TRANSISTORS) — RESULTS

BEST CIRCUIT OF GENERATION 101

X AND *Y* COORDINATES FOR OF THE 19 COMPONENTS, COMPONENT VALUE (SIZING) FOR EACH CAPACITOR AND RESISTOR, THE TYPE (*NPN* Q2N3904OR *PNP* Q2N3904) FOR EACH TRANSISTOR

Component	*X* coordinate	*Y* coordinate	Sizing / Type
Q8	-8.398678	21.184582	q2n3906
C10	-8.54565	31.121107	1.01e+02nf
R21	18.245857	-24.687471	1.48e+03k
R24	12.105233	-20.687471	5.78e+03k
R27	12.105233	-12.690355	3.61e+03k
R30	5.128666	-8.690355	8.75e+01k
R33	-3.398678	-4.690355	1.16e+03k
Q36	-3.398678	3.30961	q2n3906
Q39	-3.398678	13.309582	q2n3906
Q43	-18.472164	8.309597	q2n3904
Q45	-18.472164	-1.690355	q2n3904
Q46	-3.398678	21.184582	q2n3904
Q47	5.128666	21.184582	q2n3904
Q48	-18.472164	-17.687471	q2n3904
Q49	12.105233	21.184582	q2n3904
Q50	18.245857	21.184582	q2n3904
C52	-15.472164	31.121107	1.25e-01nf
C53	-15.472164	21.184582	7.78e+03nf
Q54	24.873787	31.121107	q2n3906