EVOLUTIONARY DESIGN OF ANALOG ELECTRICAL CIRCUITS USING GENETIC PROGRAMMING

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Abstract. The design (synthesis) of analog electrical circuits entails the creation of both the topology and sizing (numerical values) of all of the circuit's components. There has previously been no general automated technique for automatically designing an analog electrical circuit from a high-level statement of the circuit's desired behavior. This paper shows how genetic programming can be used to automate the design of both the topology and sizing of a suite of five prototypical analog circuits, including a lowpass filter, a tri-state frequency discriminator circuit, a 60 dB amplifier, a computational circuit for the square root, and a time-optimal robot controller circuit. All five of these genetically evolved circuits constitute instances of an evolutionary computation technique solving a problem that is usually thought to require human intelligence.

1. Introduction

The design process entails creation of a complex structure to satisfy user-defined requirements. The design of analog electrical circuits is particularly challenging because it is generally viewed as requiring human intelligence and because it is a major activity of practicing analog electrical engineers.

The design process for analog circuits begins with a high-level description of the circuit's desired behavior and entails creation of both the topology and the sizing of a satisfactory circuit. The topology comprises the gross number of components in the circuit, the type of each component (e.g., a resistor), and a list of all connections between the components. The sizing involves specifying the values (typically numerical) of each of the circuit's component.

Considerable progress has been made in automating the design of certain categories of purely digital circuits; however, the design of analog circuits and mixed analog-digital circuits has not proved as amenable to automation. Describing "the analog dilemma," Aaserud and Nielsen (1995) noted

> "Analog designers are few and far between. In contrast to digital design, most of the analog circuits are still handcrafted by the experts or so-called 'zahs' of analog design. The design process is characterized by a combination of experience and intuition and requires a thorough knowledge of the process characteristics and the detailed specifications of the actual product.
>
> "Analog circuit design is known to be a knowledge-intensive, multiphase, iterative task, which usually stretches over a significant period of time and is performed by designers with a large portfolio of skills. It is therefore considered by many to be a form of art rather than a science."

There has been extensive previous work on the problem of circuit design using simulated annealing, artificial intelligence, and other techniques as outlined in Koza, Bennett, Andre, Keane, and Dunlap 1997, including work using genetic algorithms (Kruiskamp and Leenaerts 1995; Grimbleby 1995; Thompson 1996). However, there has previously been no general automated technique for synthesizing an analog electrical circuit from a high-level statement of the desired behavior of the circuit. This paper presents a uniform approach to the automatic design of both the topology and sizing of analog electrical circuits.

2. Five Problems of Analog Design

This paper applies genetic programming to a suite of five problems of analog circuit design. The circuits contain a variety of types of components, including transistors, diodes, resistors, inductors, and capacitors. The circuits have varying numbers of inputs and outputs.

(1) Design a lowpass filter having one-input and one-output composed of capacitors and inductors and that passes all frequencies below 1,000 Hz and suppresses all frequencies above 2,000 Hz.

(2) Design a tri-state frequency discriminator (source identification) circuit having one input and one output that is composed of resistors, capacitors, and inductors and that produces an output of 1/2 volt and 1 volt for incoming signals whose frequencies are within 10% of 256 Hz and within 10% of 2,560 Hz, respectively, but produces an output of 0 volts otherwise.

(3) Design a computational circuit having one input and one output that is composed of transistors, diodes, resistors, and capacitors and that produces an output voltage equal to the square root of its input voltage.

(4) Design a time-optimal robot controller circuit having two inputs and one output that is composed of the above components and that navigates a constant-speed autonomous mobile robot with nonzero turning radius to an arbitrary destination in minimal time.

(5) Design an amplifier composed of the above components and that delivers amplification of 60 dB (i.e., 1,000 to 1) with low distortion and low bias.

3. Design by Genetic Programming

The circuits are developed using genetic programming (Koza 1992; Koza and Rice 1992), an extension of the genetic algorithm (Holland 1975) in which the population consists of computer programs. Multipart programs consisting of a main program and one or more reusable, parametrized, hierarchically-called subprograms can be evolved using automatically defined functions (Koza 1994a, 1994b). Architecture-altering operations (Koza 1995) automatically determine the number of such subprograms, the number of arguments that each possesses, and the nature of the hierarchical references, if any, among such automatically defined functions. For current research in genetic programming, see Kinnear 1994, Angeline and Kinnear 1996, Koza, Goldberg, Fogel, and Riolo 1996, Koza et al. 1997, and Banzhaf, Nordin, Keller, and Francone 1998.

A computer program is not a circuit. Genetic programming can be applied to designing circuits if a mapping is established between the program trees (rooted, point-labeled trees – that is, acyclic graphs – with ordered branches) used in genetic programming and the line-labeled cyclic graphs germane to electrical circuits. The principles of developmental biology, the creative work of Kitano (1990) on using genetic algorithms to evolve neural networks, and the innovative work of Gruau (1992) on using genetic programming to evolve neural networks provide motivation for a technique for mapping trees into circuits by means of a growth process that begins with an embryo. See also Brave 1996 on using genetic programming to evolve finite automata. For circuits, the embryo typically includes the inputs and outputs of the particular circuit being designed and a test harness of fixed components (such as source and load resistors). The embryo also contains modifiable wires. The embryo is a valid electrical circuit; however, until these wires are modified, the circuit does not produce interesting output. An electrical circuit is developed by progressively applying the functions in a circuit-constructing program tree to the modifiable wires of the embryo (and, during the developmental process, to new components and modifiable wires).

The functions in the circuit-constructing program trees are divided into four categories: (1) topology-modifying functions that alter the circuit topology, (2) component-creating functions that insert components into the circuit, (3) arithmetic-performing functions that appear in subtrees as argument(s) to the component-creating functions and specify the numerical value of the component, and (4) automatically defined functions that appear in the function-defining branches and potentially enable certain substructures of the circuit to be reused (with parameterization). Every program tree translates into a valid electrical circuit.

Each branch of the program tree is created in accordance with a constrained syntactic structure. Branches are composed of construction-continuing subtrees that continue the developmental process and arithmetic-performing subtrees that determine the numerical value of components. Topology-modifying functions have one or more construction-continuing subtrees, but no arithmetic-performing subtree. Component-creating functions have one or more construction-continuing subtrees and typically have one arithmetic-performing subtree. This constrained syntactic structure is preserved using structure-preserving crossover with point typing (see Koza 1994a).

3.1. The Embryonic Circuit

The starting point for the development of an electrical circuit is an embryo. The embryo is a valid (albeit useless) electrical circuit that contains at least one modifiable wire. The embryo will typically also include the input(s) and output(s) of the circuit and certain additional electrically sensible fixed components, such as a source resistor for each input and a load resistor for each output point. The specific embryo used depends on the number of inputs and outputs.

Figure 1 shows a one-input, one-output embryonic circuit in which VSOURCE is the input signal and VOUT is the output signal (the probe point). The circuit is driven by an incoming alternating circuit source VSOURCE. There is a fixed load resistor RLOAD and a fixed source resistor RSOURCE in the embryo. In addition to the fixed components, there is a modifiable wire Z0 between nodes 2 and 3. All development originates from this modifiable wire.

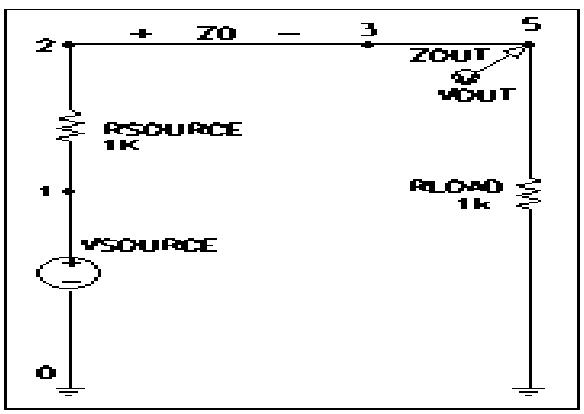

Figure 1 One-input, one-output embryo. An electrical circuit is created by executing a circuit-constructing program tree that contains various component-creating and topology-modifying functions. The population of individuals being bred by genetic programming consists of such program trees. Each tree in the population creates one circuit. The modifiable wire(s) in the embryonic circuit are transformed into various circuit components and connections as the embryo is developed into a fully developed electrical circuit by a circuit-constructing program tree. The electrical circuit is progressively developed by progressively applying the functions of the circuit-constructing program tree, in a specified orderly way, to the embryonic

circuit (and its successor circuits). After all the functions of the program tree have been executed, the developmental process is completed and the result is a fully developed electrical circuit.

3.2. Component-Creating Functions

Each program tree contains component-creating functions and topology-modifying functions. The component-creating functions insert a component into the developing circuit and assign component value(s) to the component.

Each component-creating function has a writing head that points to an associated component in the developing circuit and modifies that component in a specified manner. The construction-continuing subtree of each component-creating functions points to a successor function or terminal in the circuit-constructing program tree.

The arithmetic-performing subtree of a component-creating functions consists of a composition of arithmetic functions (addition and subtraction) and random constants (in the range -1.000 to +1.000). The arithmetic-performing subtree specifies the numerical value of a component by returning a floating-point value that is interpreted on a logarithmic scale as the value for the component in a range of 10 orders of magnitude (using a unit of measure that is appropriate for the particular type of component.

The two-argument resistor-creating R function causes the highlighted component to be changed into a resistor. The value of the resistor in kilo Ohms specified by its arithmetic-performing subtree.

The left part of figure 2 shows a modifiable wire Z0 connecting nodes 1 and 2 of a partial circuit containing four capacitors (C2, C3, C4, and C5). The circle indicates that Z0 has a writing head (i.e., is the highlighted component and that Z0 is subject to subsequent modification). The right part of the figure shows the result of applying the R function to Z0. The circle indicates that the newly created R1 has a writing head R1 and thus remains subject to subsequent modification.

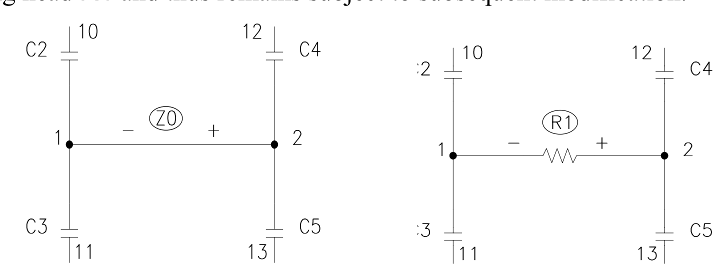

Figure 2 (a) Modifiable wire Z0. (b) Result of R function.

Similarly, the two-argument capacitor-creating C function causes the highlighted component to be changed into a capacitor whose value in micro Farads is specified by the arithmetic-performing subtrees.

The one-argument Q_D_PNP diode-creating function causes a diode to be inserted in lieu of the highlighted component. This function has only one argument because there is no numerical value associated with a diode and thus no arithmetic-performing subtree. In practice, the diode is implemented here using a pnp transistor whose collector and base are connected to each other. The Q_D_NPN function inserts a diode using an npn transistor in a similar manner.

There are also six one-argument transistor-creating functions (Q_POS_COLL_NPN, Q_GND_EMIT_NPN, Q_NEG_EMIT_NPN, Q_GND_EMIT_PNP, Q_POS_EMIT_PNP, Q_NEG_COLL_PNP) that insert a bipolar junction transistor in lieu of the highlighted component and that directly connect the collector or emitter of the newly created transistor to a fixed point of the circuit (the positive power supply, ground, or the negative power supply). For example, the Q_POS_COLL_NPN function inserts a bipolar junction transistor whose collector is connected to the positive power supply.

Each of the functions in the family of six different three-argument transistor-creating Q_3_NPN functions causes an npn bipolar junction transistor to be inserted in place of the highlighted component and one of the nodes to which the highlighted component is connected. The Q_3_NPN function creates five new nodes and three modifiable wires. There is no writing head on the new transistor, but there is a writing head on each of the three new modifiable wires. There are 12 members (called Q_3_NPN0, ..., Q_3_NPN11) in this family of functions because there are two choices of nodes (1 and 2) to be bifurcated and then there are six ways of attaching the transistor's base, collector, and emitter after the bifurcation. Similarly the family of 12 Q_3_PNP functions inserts a pnp bipolar junction transistor.

3.3. Topology-Modifying Functions

Each topology-modifying function in a program tree points to an associated highlighted component and modifies the topology of the developing circuit.

The three-argument SERIES division function creates a series composition of the highlighted component (with a writing head), a copy of it (with a writing head), one new modifiable wire (with a writing head), and two new nodes.

The four-argument PSS parallel division function creates a parallel composition consisting of the original highlighted component (with a writing head), a copy of it (with a writing head), two new modifiable wires (each with a writing head), and two new nodes. Figure 3 shows the result of applying PSS to resistor R1 of figure 2a.

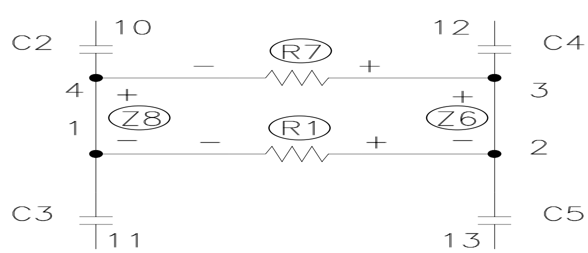

Figure 3 Result of the PSS function. The one-argument polarity-reversing FLIP function reverses the polarity of the highlighted component.

There are six three-argument functions (T_GND_0, T_GND_1, T_POS_0, T_POS_1, T_NEG_0, T_NEG_1) that insert two new nodes and two new modifiable wires, and then make a connection to ground, positive power supply, or negative power supply, respectively.

There are two three-argument functions (PAIR_CONNECT_0 and PAIR_CONNECT_1) that enable distant parts of a circuit to be connected together. The first PAIR_CONNECT to occur in the development of a circuit creates two new wires, two new nodes, and one temporary port. The next `PAIR_CONNECT` creates two new wires and one new node, connects the temporary port to the end of one of these new wires, and then removes the temporary port.

The one-argument `NOOP` function has no effect on the highlighted component; however, it delays activity on the developmental path on which it appears in relation to other developmental paths in the overall program tree.

The zero-argument `END` function causes the highlighted component to lose its writing head, thereby ending that particular developmental path.

The zero-argument `SAFE_CUT` function causes the highlighted component to be removed from the circuit provided that the degree of the nodes at both ends of the highlighted component is three (i.e., no dangling components or wires are created).

4. Preparatory Steps

Before applying genetic programming to a problem of circuit design, seven major preparatory steps are required: (1) identify the suitable embryonic circuit, (2) determine the architecture of the overall circuit-constructing program trees, (3) identify the terminals of the program trees, (4) identify the primitive functions contained in these program trees, (5) create the fitness measure, (6) choose parameters, and (7) determine the termination criterion and method of result designation.

4.1. Embryonic Circuit

The embryonic circuit used on a particular problem depends on the circuit's number of inputs and outputs. For example, the one-input, one-output embryo (figure 1) was used for the lowpass filter. However, the robot controller circuit has two inputs and both inputs need their own separate source resistors. Moreover, the embryo has three modifiable wires in order to provide full connectivity between the two inputs and the one output. In some problems, such as the amplifier, the embryo contains additional fixed components because of additional problem-specific functionality of the test harness.

4.2. Program Architecture

Since there is one result-producing branch in the program tree for each modifiable wire in the embryo, the architecture of each circuit-constructing program tree depends on the embryonic circuit. One result-producing branch was used for the frequency discriminator and the computational circuit; two were used for lowpass filter problem; and three were used for the robot controller and amplifier. The architecture of each circuit-constructing program tree also depends on the use, if any, of automatically defined functions. Automatically defined functions and architecture-altering operations were used in the frequency discriminator, robot controller, and amplifier. For these problems, each program tree in the initial random population of programs had a uniform architecture with no automatically defined functions. In later generations, the number of automatically defined functions, if any, emerged as a consequence of the architecture-altering operations.

4.3. Function and Terminal Sets

The function set for each design problem depended on the type of electrical components that were used to construct the circuit. Capacitors, diodes, and transistors were used for the computational circuit, the robot controller, and the amplifier. Resistors were used for the frequency discriminator. When transistors were used, functions to provide connectivity to the positive and negative power supplies were also included,.

For the computational circuit, the robot controller, and the amplifier, the function set, $\mathcal{F}_{\text{ccs-initial}}$, for each construction-continuing subtree was

$\mathcal{F}_{\text{ccs-initial}}$ = {`R`, `C`, `SERIES`, `PSS`, `PSL`, `FLIP`, `NOOP`, `T_GND_0`, `T_GND_1`, `T_POS_0`, `T_POS_1`, `T_NEG_0`, `T_NEG_1`, `PAIR_CONNECT_0`, `PAIR_CONNECT_1`, `Q_D_NPN`, `Q_D_PNP`, `Q_3_NPN0`, ..., `Q_3_NPN11`, `Q_3_PNP0`, ..., `Q_3_PNP11`, `Q_POS_COLL_NPN`, `Q_GND_EMIT_NPN`, `Q_NEG_EMIT_NPN`, `Q_GND_EMIT_PNP`, `Q_POS_EMIT_PNP`, `Q_NEG_COLL_PNP`}.

For the npn transistors, the `Q2N3904` model was used. For pnp transistors, the `Q2N3906` model was used.

The initial terminal set, $\mathcal{T}_{\text{ccs-initial}}$, for each construction-continuing subtree was

$\mathcal{T}_{\text{ccs-initial}}$ = {`END`, `SAFE_CUT`}.

The initial terminal set, $\mathcal{T}_{\text{aps-initial}}$, for each arithmetic-performing subtree consisted of

$\mathcal{T}_{\text{aps-initial}} = \{\leftarrow\}$,

where $\leftarrow$ represents floating-point random constants from –1.0 to +1.0.

The function set, $\mathcal{F}_{\text{aps}}$, for each arithmetic-performing subtree was,

$\mathcal{F}_{\text{aps}}$ = {`+`, `-`}.

The terminal and function sets were identical for all result-producing branches for a particular problem.

For the lowpass filter and frequency discriminator, there was no need for functions to provide connectivity to the positive and negative power supplies.

For the frequency discriminator, the robot controller, and the amplifier, the architecture-altering operations were used and the set of potential new functions, $\mathcal{F}_{\text{potential}}$, was

$\mathcal{F}_{\text{potential}}$ = {`ADF0`, `ADF1`, ...}.

The set of potential new terminals, $\mathcal{T}_{\text{potential}}$, for the automatically defined functions was

$\mathcal{T}_{\text{potential}}$ = {`ARG0`}.

The architecture-altering operations changed the function set, $\mathcal{F}_{\text{ccs}}$ for each construction-continuing subtree of all three result-producing branches and the function-defining branches, so that

$\mathcal{F}_{\text{ccs}} = \mathcal{F}_{\text{ccs-initial}} \approx \mathcal{F}_{\text{potential}}$.

The architecture-altering operations generally changed the terminal set for automatically defined functions, $\mathcal{T}_{\text{aps-adf}}$, for each arithmetic-performing subtree, so that

$$\mathcal{T}_{\text{aps-adf}} = \mathcal{T}_{\text{aps-initial}} \approx \mathcal{T}_{\text{potential}}.$$

4.4. Fitness Measure

The fitness measure varies for each problem. The high-level statement of desired circuit behavior is translated into a well-defined measurable quantity that can be used by genetic programming to guide the evolutionary process. The evaluation of each individual circuit-constructing program tree in the population begins with its execution. This execution progressively applies the functions in each program tree to an embryonic circuit, thereby creating a fully developed circuit. A netlist is created that identifies each component of the developed circuit, the nodes to which each component is connected, and the value of each component. The netlist becomes the input to the 217,000-line SPICE (Simulation Program with Integrated Circuit Emphasis) simulation program (Quarles, Newton, Pederson, and Sangiovanni-Vincentelli 1994). SPICE then determines the behavior of the circuit. It was necessary to make considerable modifications in SPICE so that it could run as a submodule within the genetic programming system.

4.4.1 Lowpass Filter

A simple *filter* is a one-input, one-output electronic circuit that receives a signal as its input and passes the frequency components of the incoming signal that lie in a specified range (called the *passband*) while suppressing the frequency components that lie in all other frequency ranges (the *stopband*).

The desired lowpass LC filter should have a passband below 1,000 Hz and a stopband above 2,000 Hz. The circuit is driven by an incoming AC voltage source with a 2 volt amplitude. If the source (internal) resistance RSOURCE and the load resistance RLOAD in the embryonic circuit are each 1 kilo Ohm, the incoming 2 volt signal is divided in half.

The *attenuation* of the filter is defined in terms of the maximum signal in its stopband relative to the reference voltage (half of 2 volt here). A *decibel* is a unitless measure of relative voltage that is defined as 20 times the common (base 10) logarithm of the ratio between the voltage at a particular probe point and a reference voltage.

A voltage in the passband of exactly 1 volt and a voltage in the stopband of exactly 0 volts are considered ideal. A voltage in the passband of between 970 millivolts and 1 volt and a voltage in the stopband of between 0 volts and 1 millivolt are regarded as acceptable. The (preferably small) shortfall from 1 volt in the passband is called the *passband attenuation*. Similarly, the (preferably small) signal in the stopband is called the *stopband attenuation*. Any voltage lower than 970 millivolts in the passband and any voltage above 1 millivolts in the stopband is regarded as unacceptable. A fifth-order *elliptic* (*Cauer*) *filter* with a modular angle Θ of 30 degrees (i.e., the arcsin of the ratio of the boundaries of the passband and stopband) and a reflection coefficient ρ of 20% satisifes these design goals.

Since the high-level statement of behavior for the desired circuit is expressed in terms of frequencies, the voltage VOUT is measured in the frequency domain. SPICE performs an AC small signal analysis and report the circuit's behavior over five decades (between 1 Hz and 100,000 Hz) with each decade being divided into 20 parts (using a logarithmic scale),so that there are a total of 101 fitness cases.

Fitness is measured in terms of the sum over these cases of the absolute weighted deviation between the actual value of the voltage that is produced by the circuit at the probe point VOUT and the target value for voltage. The smaller the value of fitness, the better. A fitness of zero represents an (unattainable) ideal filter.

Specifically, the standardized fitness is

$$F(t) = \sum_{i=0}^{100} \left(W(d(f_i), f_i) d(f_i) \right)$$

where f_i is the frequency of fitness case i; $d(x)$ is the absolute value of the difference between the target and observed values at frequency x; and $W(y,x)$ is the weighting for difference y at frequency x.

The fitness measure is designed to not penalize ideal values, to slightly penalize every acceptable deviation, and to heavily penalize every unacceptable deviation. Specifically, the procedure for each of the 61 points in the 3-decade interval between 1 Hz and 1,000 Hz is as follows: If the voltage equals the ideal value of 1.0 volt in this interval, the deviation is 0.0. If the voltage is between 970 millivolts and 1 volt, the absolute value of the deviation from 1 volt is weighted by a factor of 1.0. If the voltage is less than 970 millivolts, the absolute value of the deviation from 1 volt is weighted by a factor of 10.0. The acceptable and unacceptable deviations for each of the 35 points from 2,000 Hz to 100,000 Hz are similarly weighed (by 1.0 or 10.0).

For each of the five "don't care" points between 1,000 and 2,000 Hz, the deviation is deemed to be zero.

The number of “hits” for this problem (and all other problems herein) is defined as the number of fitness cases for which the voltage is acceptable or ideal or that lie in the "don't care" band (for a filter).

Many of the random initial circuits and many that are created by the crossover and mutation operations in subsequent generations cannot be simulated by SPICE. These circuits receive a high penalty value of fitness (10^8) and become the worst-of-generation programs for each generation.

4.4.2 Tri-state Frequency Discriminator

Fitness is the sum, over 101 fitness cases, of the absolute weighted deviation between the actual value of the voltage that is produced by the circuit and the target value.

The three points that are closest to the band located within 10% of 256 Hz are 229.1 Hz, 251.2 Hz, and 275.4 Hz. The procedure for each of these three points is as follows: If the voltage equals the ideal value of 1/2 volts in this interval, the deviation is 0.0. If the voltage is more than 240 millivolts from 1/2 volts, the absolute value of the deviation from 1/2 volts is weighted by a factor of 20. If the voltage is more than 240 millivolts of 1/2 volts, the absolute value of the deviation from 1/2 volts is weighted by a factor of 200. This arrangement reflects the fact that the ideal output voltage for this range of frequencies is 1/2 volts, the fact that a 240 millivolts discrepancy is acceptable, and the fact that a larger discrepancy is not acceptable.

Similar weighting was used for the three points (2,291 Hz, 2,512 Hz, and 2,754 Hz) that are closest to the band located within 10% of 2,560 ,Hz.

The procedure for each of the remaining 95 points is as follows: If the voltage equals the ideal value of 0 volts, the deviation is 0.0. If the voltage is within 240 millivolts of 0 volts, the absolute value of the deviation from 0 volts is weighted by a factor of 1.0. If the voltage is more than 240 millivolts from 0 volts, the absolute value of the deviation from 0 volts is weighted by a factor of 10. For details, see Koza, Bennett, Lohn, Dunlap, Andre, and Keane 1997b.

4.4.3 Computational Circuit

SPICE is called to perform a DC sweep analysis at 21 equidistant voltages between –250 millivolts and +250 millivolts. Fitness is the sum, over these 21 fitness cases, of the absolute weighted deviation between the actual value of the voltage that is produced by the circuit and the target value for voltage. For details, see Koza, Bennett, Lohn, Dunlap, Andre, and Keane 1997a.

4.4.4 Robot Controller Circuit

The fitness of a robot controller was evaluated using 72 randomly chosen fitness cases each representing a different target point. Fitness is the sum, over the 72 fitness cases, of the travel times. If the robot came within a capture radius of 0.28 meters of its target point before the end of the 80 time steps allowed for a particular fitness case, the contribution to fitness for that fitness case was the actual time. However, if the robot failed to come within the capture radius during the 80 time steps, the contribution to fitness was 0.160 hours (i.e., double the worst possible time).

SPICE performs a nested DC sweep, which provides a way to simulate the DC behavior of a circuit with two inputs. It resembles a nested pair of `FOR` loops in a computer program in that both of the loops have a starting value for the voltage, an increment, and an ending value for the voltage. For each voltage value in the outer loop, the inner loop simulates the behavior of the circuit by stepping through its range of voltages. Specifically, the starting value for voltage is –4 volt, the step size is 0.2 volt, and the ending value is +4 volt. These values correspond to the dimensions of the robot's world of 64 square meters extending 4 meters in each of the four directions from the origin of a coordinate system (i.e., 1 volt equals 1 meter). For details, see Koza, Bennett, Keane, and Andre 1997.

4.4.5 60 dB Amplifier

SPICE was requested to perform a DC sweep analysis to determine the circuit's response for several different DC input voltages. An ideal inverting amplifier circuit would receive the DC input, invert it, and multiply it by the amplification factor. A circuit is flawed to the extent that it does not achieve the desired amplification, the output signal is not perfectly centered on 0 volts(i.e., it is biased), or the DC response is not linear. Fitness is calculated by summing an amplification penalty, a bias penalty, and two non-linearity penalties – each derived from these five DC outputs. For details, see Bennett, Koza, Andre, and Keane 1996.

4.5. Control Parameters

The population size, *M*, was 640,000 for all problems. Other parameters were substantially the same for each of the five problems and can be found in the references cited above.

4.6. Implementation on Parallel Computer

Each problem was run on a medium-grained parallel Parsytec computer system (Andre and Koza 1996) consisting of 64 80-MHz PowerPC 601 processors arranged in an 8 by 8 toroidal mesh with a host PC Pentium type computer. The distributed genetic algorithm was used with a population size of Q = 10,000 at each of the D = 64 demes (semi-isolated subpopulations). On each generation, four boatloads of emigrants, each consisting of B = 2% (the migration rate) of the node's subpopulation (selected on the basis of fitness) were dispatched to each of the four adjacent processing nodes.

5. Results

In all five problems, fitness was observed to improve over successive generations. Satisfactory results were generated in every case on the first or second run. When two runs were required, the first produced an almost satisfactory result.

5.1. Lowpass Filter

Many of the runs produced lowpass filters having a topology similar to that employed by human engineers. For example, in generation 32 of one run, a circuit (figure 4) was evolved with a near-zero fitness of 0.00781. The circuit was 100% compliant with the design requirements in that it scored 101 hits (out of 101). This circuit had the recognizable ladder topology (46) of a Butterworth or Chebychev filter (i.e., a composition of series inductors horizontally with capacitors as vertical shunts).

Figure 5 shows the behavior in the frequency domain of this evolved lowpass filter. As can be seen, the evolved circuit delivers about 1 volt for all frequencies up to 1,000 Hz and about 0 volts for all frequencies above 2,000 Hz.

In another run, a 100% compliant recognizable "bridged T" arrangement was evolved. In yet another run using automatically defined functions, a 100% compliant circuit emerged with the recognizable elliptic topology that was invented and patented by Cauer. When invented, the Cauer filter was a significant advance (both theoretically and commercially) over the Butterworth and Chebychev filters.

Thus, genetic programming rediscovered the ladder topology of the Butterworth and Chebychev filters, the "bridged T" topology, and the elliptic topology.

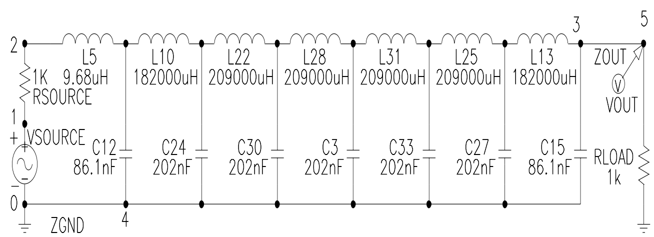

Figure 4 Evolved 7-rung ladder filter.

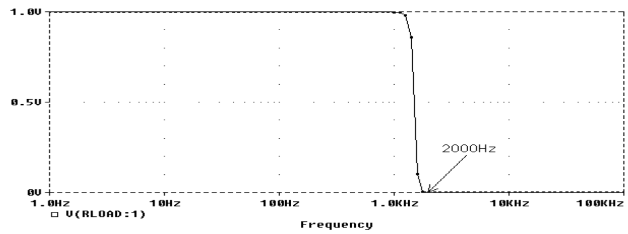

Figure 5 Frequency domain behavior of evolved 7-rung ladder filter.

5.2. Tri-state Frequency Discriminator

The evolved three-way tri-state frequency discriminator circuit from generation 106 scores 101 hits (out of 101). Figure 6 shows this circuit (after expansion of its automatically defined functions). The circuit produces the desired outputs of 1 volt and 1/2 volts (each within the allowable tolerance) for the two specified bands of frequencies and the desired near-zero signal for all other frequencies.

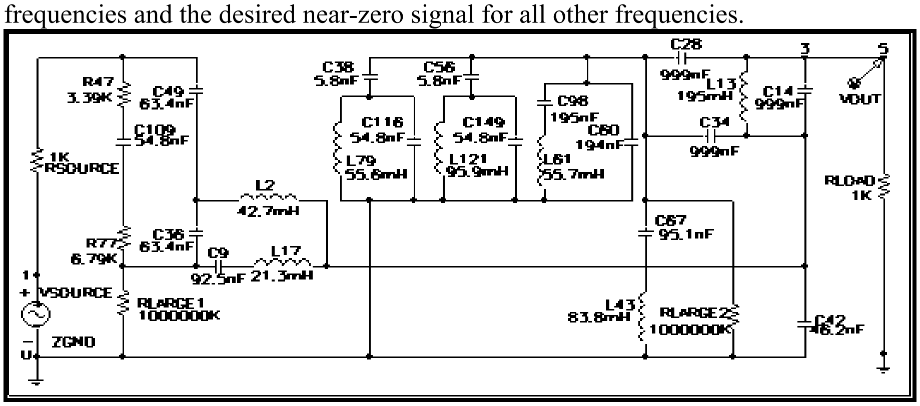

Figure 6 Evolved frequency discriminator.

5.3. Computational Circuit

The genetically evolved computational circuit for the square root from generation 60 (figure 7), achieves a fitness of 1.68, and has 36 transistors, two diodes, no capacitors, and 12 resistors (in addition to the source and load resistors in the embryo). The output voltages produced by this best-of-run circuit are almost exactly the required values.

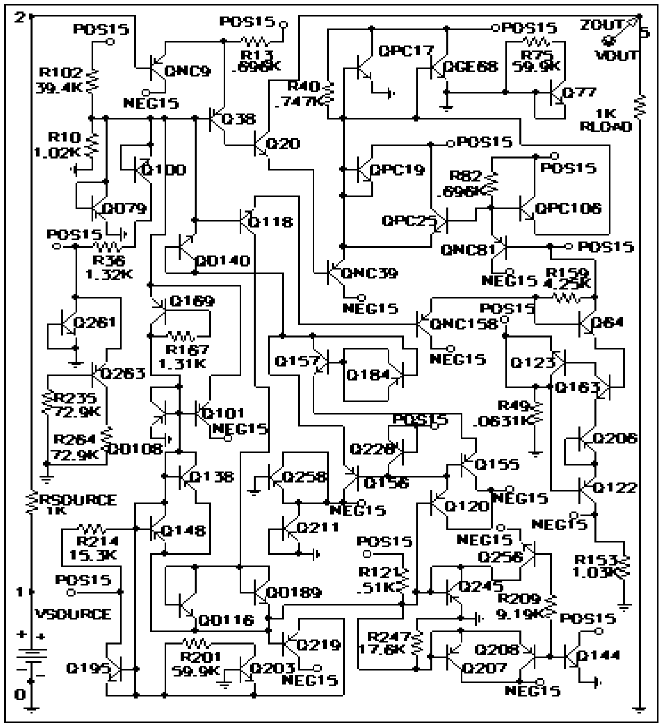

Figure 7 Evolved square root circuit.

5.4. Robot Controller Circuit

The best-of-run time-optimal robot controller circuit (figure 8) appeared in generation 31, scores 72 hits, and achieves a near-optimal fitness of 1.541 hours. In comparison, the optimal value of fitness for this problem is known to be 1.518 hours. This best-of-run circuit has 10 transistors and 4 resistors. The program has one automatically defined function that is called twice (incorporated into the figure).

5.5. 60 dB Amplifier

The best circuit from generation 109 (figure 9) achieves a fitness of 0.178. Based on a DC sweep, the amplification is 60 dB here (i.e., 1,000-to-1 ratio) and the bias is 0.2 volt. Based on a transient analysis at 1,000 Hz, the amplification is 59.7 dB; the bias is 0.18 volts; and the distortion is very low (0.17%). Based on an AC sweep, the amplification at 1,000 Hz is 59.7 dB; the flatband gain is 60 dB; and the 3 dB bandwidth is 79, 333 Hz. Thus, a high-gain amplifier with low distortion and acceptable bias has been evolved.

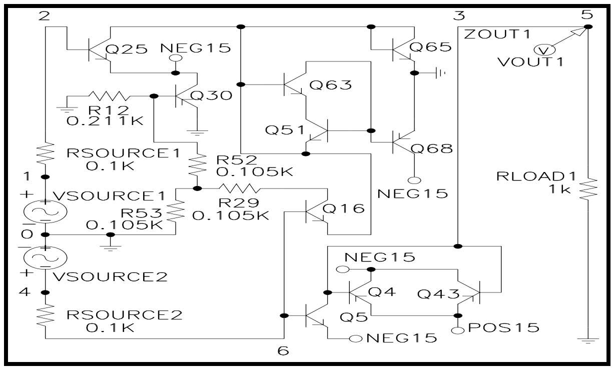

Figure 8 Evolved robot controller.

6. Other Circuits

Numerous other circuits have been similarly designed, including an asymmetric bandpass filter, crossover filter, comb filter, amplifier, temperature-sensing circuit, and voltage reference circui (Koza, Bennett, Andre, and Keane 1996; Koza, Andre, Bennett, and Keane 1996; and Koza, Bennett, Andre, Keane, and Dunlap 1997; Bennett 1997).

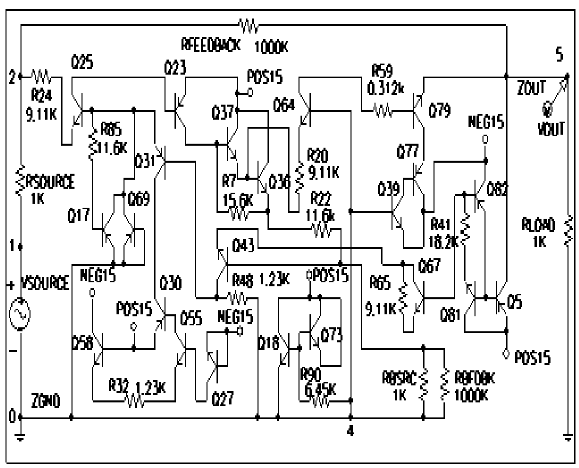

Figure 9 Genetically evolved amplifier.

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EVOLUTIONARY DESIGN OF ANALOG ELECTRICAL CIRCUITS USING GENETIC PROGRAMMING

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